AMENDMENTS TO THE SPECIFICATION:

1. Please amend the paragraph beginning on page 57, line 25, and ending on page 58, line 3, as follows:

After the step shown in FIG. 16O, the W film 113, now the gate wiring layer 113GW, is etched back by RIE or SH processing, as shown in FIG. 16U. As shown in FIG. 16V, a silicon nitride film 137 is formed and flattened by CMP or resist etch-back. This flattening is performed until the polysilicon film 111 is exposed.

2. Please amend the paragraph beginning on page 58, line 11, and ending on page 59, line 8, as follows:

In FIG. 16X, an insulating film 138 such as a silicon oxide film is formed on the MOSFET shown in FIG. 16W. To form an opening in the insulating film 138 in order to connect the source/drain electrode, a resist film (not shown) must be formed on the insulating film 138 by lithography. For example, when misalignment occurs, an opening may also be formed in the insulating film 138 above the gate electrode 113GE. In this case, if the opening of the insulating film 138 is filled with a metal 139 such as Al, the gate electrode 113GE may be electrically short-circuited with the source/drain electrode 135. To the contrary, as shown in FIG. 16X, when the silicon nitride film 137 is formed on only the gate electrode 113GE, the gate electrode is covered with the silicon nitride film 137. Therefore, even if the opening is filled with the metal 139, the gate electrode 113GE, is not electrically short-circuited with the source/drain electrode 135. In addition, the gate insulating film 132 made of a silicon oxide film is partially etched upon forming the opening. However, since the upper surface of the gate electrode is at a

position lower than the upper surface of the source/drain electrode, the opening can be formed without excessively etching the gate insulating film 132.